*The 2012 World Congress on*
***Advances in Civil, Environmental, and Materials Research (ACEM' 12)***
*Seoul, Korea, August 26-30, 2012*

# Simulation of a Novel Piezoelectric Energy Harvester

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## ABSTRACT

This paper focuses on a novel piezoelectric energy harvester for nanofiber PVDF to capture energy from vibration environment. A Resembling CMOS(R-CMOS) circuit consisting of two pMOS transistors and two nMOS transistors is presented, which can greatly increase the energy efficiency and reduce the power dissipation tremendously. Meanwhile, the novel harvester supplies smooth direct current. Simulation result of MULTISIM has shown that by using this novel piezoelectric energy harvester the input voltage (5v) can be rectified to be an output voltage (4.24v). The voltage conversion rate of the novel harvester is as high as 84.8% which is much larger than the rate of traditional rectifier circuit. Its potential application is in micro sensors, wireless transducers, and sensor networks.

## 1. INTRODUCTION

With the development of micro sensor and low-power device, there is a growing need for a green, high-efficiency and reliable power supply. The conventional electrochemical battery which has a large size, a short battery life and a high replacement cost can't meet the demand and people try to find a new type of generator. As the piezoelectric material that can convert vibration energy into electrical energy has the advantages of simple structure, huge energy density, and long life cycle and free of electromagnetic interference, the piezoelectric energy harvesting has been a promising energy harvesting technology. (Guilar 2009) have pointed that the piezoelectric energy harvester (PEH) has been a viable way to supply wireless system without batteries. In this paper, the novel PEH is designed based on the nano-fiber PVDF that is developed by Tong Lin in Deakin University. This new piezoelectric material has a lower power loss, high and table Electrical outputs than traditional piezoelectric materials. That is why this material is chosen.

In recent years, some researchers have done a wide range of research on the energy converter circuit to improve the PEH efficiency. (Soobu 2011) have done much

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work about PEH. (Junrui 2012) have suggested that the traditional rectifier contains a diode Wien Bridge to change alternating current (AC) to direct current (DC). However, it has a low power conversion efficiency (PCE) and a high power loss. Many researchers tried to change the successive storage capacitor to increase the PCE and the signal bandwidth. (Florentino 2011) have used a variable capacitor and a piezoelectric transducer to construct a simple circuit module which can provide DC power while compensate the leakage loss of the capacitor. (Xuan-Dien 2011) have employed two synchronous to improve the traditional rectifier which doubles the PCE. Furthermore, the output is connected with LDO to improve the whole energy harvesting effect. (Lallart 2008) have used several discrete components to design a self-powered SSHI interface circuit which increases the PCE by 1.6 times. (Junwu 2011) have found that the cascade of rectifying bridge can increase the output voltage and frequency bandwidth of the multi-oscillator generator. Although these methods have improved the harvesting effects to certain degrees, the complexity of the circuit determines the heavy power loss. Moreover, the power loss of the traditional piezoelectric material is huge which decreases the PCE of the whole harvesting system.

The nano-fiber PVDF developed by Tong Lin in Deakin University can produce a high voltage output when it operates in a low frequency. MOS transistor has high power conversion efficiency, simple structure and low power consumption. So in this paper, a Resembling CMOS(R-CMOS) circuit is presented which is composed of four MOS transistors. Based on the characteristic of the R-CMOS, a better output features than the typical circuit by using the nano-fiber PVDF can be obtained. With a low power loss and a high output voltage, this novel harvester can provide power for wireless transducers and micro sensors.

The remainder of this paper is organized as follows. Section II introduces the working principles of typical PEH and our R-CMOS rectifier circuit. In Section III, the low power advantage of the R-CMOS has been justified by the formula derivation and the fact of the comparison with the typical and the synchronous switch circuit. Section IV gives the result of the simulation. At last the whole paper is concluded.

## 2. PRINCIPLE OF TYPICAL HARVESTER AND THE NOVEL ONE

A piezoelectric energy harvester contains four main components as Fig. 1.

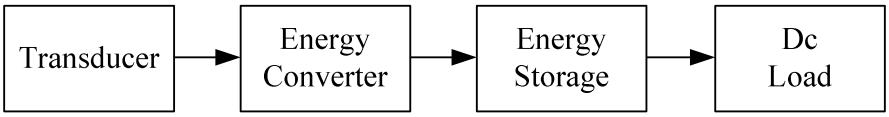


Fig. 1. Schematic diagram of the PEH

The transducer converts the ambient vibration energy into electrical energy which is strong and irregular function of time. Usually, we can’t use this power directly, just as the views in (D’hulst 2010). So we put a energy converter (rectifier) after it to produce a DC supply source. Then the direct current is stored in a big capacitor or nickel metal hydride rechargeable battery, which is used to drive the DC load. The energy converter is a very important link and largely determines the efficiency of energy transformation. With different rectifier, the efficiency of PEH is quite different.

## 2.1. Typical piezoelectric energy harvester

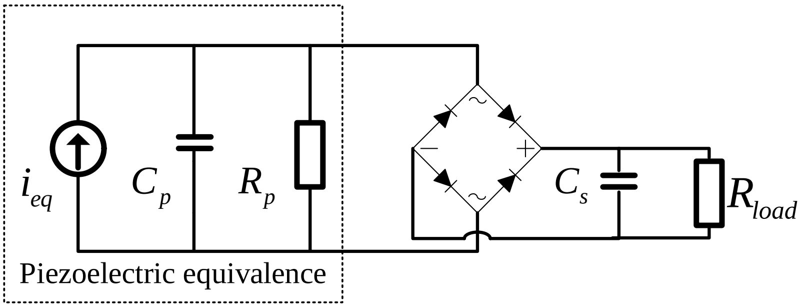


Fig. 2. Equivalent circuit of the typical PEH

Given a typical PEH device, e.g., a piezoelectric cantilever with harvesting interface circuit and energy storage, the Equivalent circuit of the typical PEH could express by Fig. 2. in (Junrui 2012), the piezoelectric structure in the circuit is modeled as an equivalent current source $i_{eq}$ in parallel with the piezoelectric clamped Capacitance $C_p$ and the internal leakage resistance $R_p$. The current source $i_{eq}$ is proportional to the vibration velocity $\dot{x}$ with the relation of

$$i_{eq}(t) = \alpha_e \dot{x}(t) \tag{1}$$

Where $\alpha_e$ is the force-voltage factor of the piezoelectric structure in Eq. (1). A full bridge rectifier is used as the energy converter, and its dc flow is stored in a cap.

## 2.2. Piezoelectric energy harvester with the Resembling-CMOS rectifier

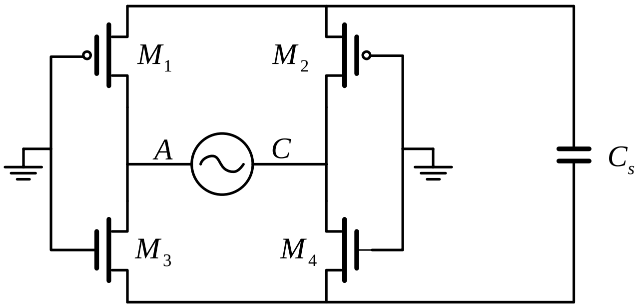


Fig. 3. Piezoelectric energy harvester with the R-CMOS rectifier

In the typical piezoelectric energy harvester, the full bridge rectifier of diode is used to rectify the AC. With high forward drop and power dissipation, it is not quite suit for the low-voltage application. To enhance the efficiency, we propose the R-CMOS rectifier which consists of two pMOS transistors （$M_1$、$M_2$） and two nMOS transistors ($M_3$、$M_4$), see in Fig. 3. (Xuan-Dien 2011) have indicated that the pMOS rectifier reduce drop voltage of two passive diode from thread voltage of diode (about 0.5-0.7v) to the voltage of pMOS ($Vds \approx 5mv$).The remain nMOS also significant reduces drop voltage. With a good rectify efficiency, the R-CMOS rectifier has a lower consumption. The consumption analysis of R-CMOS is discussed in part 3.

In Fig. 3, the transducer is modeled as a sinusoidal source. When port A of the source put a positive level, we can get $Vgs_{1、3} < 0$，$Vgs_{2、4} > 0$. With the increase of voltage, $M_1$ and $M_4$ are gradually turned on. The $V_{C_s}$ is charged up via $M_1$、$C$、and $M_4$. The operation of the rectifier is similar to that of the first half-period when the port A gives a negative level.

## 3. POWER ANALYSIS OF THE R-CMOS

Operating at 10Hz the average output voltage and current of the new piezoelectric nano-fiber ($2cm^2$) is 6v and $5\mu A$ respectively, which demonstrates that the nano-fiber has a high output voltage and a relatively low output current, and the average power provided by the nano-fiber is $30\mu W$. In order to obtain a low loss output voltage, the low loss MOS transistors are used to bring down the power loss of the whole harvester circuit.

The no-load loss of Transistor-Transistor Logic (TTL) circuit is much heavier than CMOS circuit, while the former is at the grade of milli-warts and the latter is just at nano-warts. The novel harvester in this paper mainly consists of a Resembling CMOS (R-CMOS) circuit which includes two N type enhancement mode MOS transistors and two P type enhancement mode transistors. The power loss of CMOS circuit generates from leakage power consumption, short circuit power consumption, charging and discharging power consumption. Leakage power consumption is led by the leakage currents. Short circuit power consumption generates when the currents flow from the circuit to the ground due to the variation of the output voltage. This paper mainly discusses the charging and discharging power consumption because the former two ones are much smaller than the last one. The charging and discharging power consumption generates from the charging and discharging process of the load capacitance due to the variation of the output logic level. (Xinmin 2000) have suggested the formula of this consumption.

$$p = \frac{1}{T}\left[\int_0^{\frac{T}{2}} i_N \cdot U \cdot dt + \int_{\frac{T}{2}}^{T} i_P (U_d - U_o) \cdot dt\right] \tag{2}$$

Where $T$: period of input pulses

$i_N$ : discharging current of N type MOS transistor

$i_P$ : charging current of P type MOS transistor

$U_o$ : output voltage

$U_d$ : supply voltage

Consuming that the N type and P type MOS transistors have the same electrical parameters, then $i_N = i_P = i_o$ , meanwhile $i_o = C \cdot \frac{dU_o(t)}{dt}$ .

Then Eq. (2) can be written like this.

$$p = \frac{1}{T} \cdot C \cdot U_d^2 = f \cdot C \cdot U_d^2 \tag{3}$$

Where $C$ : total capacitance of the MOS transistor

As in practical application, the grid capacitance of the MOS transistor changes with the condition of the channel. While under the switch-on working condition of the electronic circuit, the MOS transistor can pass through the capacitance transition region very quickly. Then C in Eq. (3) approximates the capacitance of the thin gate oxide between the grid and the channel conductive layer, which can be written as Eq. (4).

$$C = C_o = \frac{\varepsilon_o * \varepsilon_{ox} * (L \cdot W)}{t_{ox}} \tag{4}$$

Where $\varepsilon_o$ : permittivity of vacuum

$\varepsilon_{ox}$ : relative permittivity of $SiO_2$

$t_{ox}$ : length of the $SiO_2$ layer

$L$ : channel length of the MOS transistor

$W$ : channel width of the MOS transistor

This paper uses the $0.35\mu m$ fabricated MOS transistor whose channel length, channel width and length of the silicon dioxide is $10\mu m$ , $1000\mu m$ and $5nm$ respectively. Then the $C$ in Eq. (4) is $68.64pf$ and the power loss is $0.025\mu W$ , which is much smaller than $30\mu W$ .

The typical PEH consists of four diodes which are seen in Fig. 4.

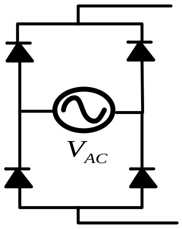


Fig. 4. Wien's bridge diodes

If the low loss Schottky diodes (with a low forward drop of 0.3v) are used in The typical PEH and the current of one period is $5\mu A$, then the power loss is $6\mu W$, which is much heavier than the novel harvester in this paper ($0.025\mu W$).

The synchronous switch circuit designed by Korean Advanced Institute of Science and Technology is shown in Fig.5.

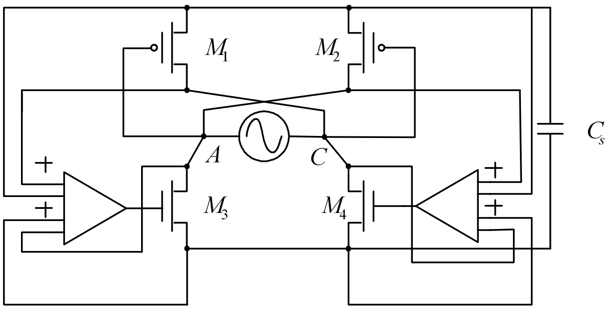


Fig. 5. Synchronous switch circuit

This synchronous switch circuit employs two additional comparators which results in a heavier power loss than the novel harvester of this paper.

## 4. SIMULATION RESULTS OF TYPICAL CIRCUIT AND THE R-CMOS

Simulation of the novel harvester is based on the Multisim 10.0 platform. Multisim is an outstanding simulation tool produced by National Instruments of America which is based on Windows operating system. It has a variety of simulation and analysis functions, including circuit schematics input and Very-High-Speed Integrated Circuit Hardware Description Language (VHDL) input.

The signal source used in our research is as follows which simulates the output signal of the novel nano-fiber.

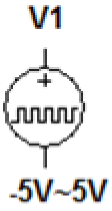


Fig. 6. Signal source

The following figure from the *Centr*e for Material and Fibre Innovation of Deakin University shows the output voltage of the nano-fiber ($2cm^2$) when operating at 1 Hz, 5 Hz and 10 Hz respectively.

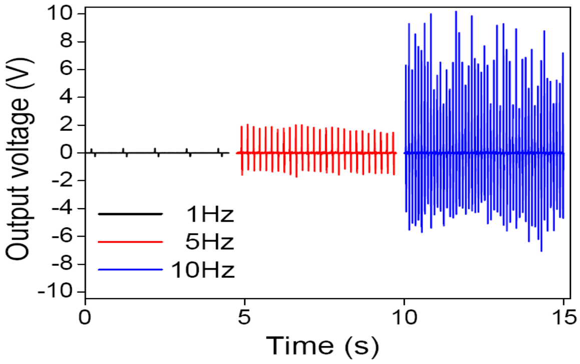


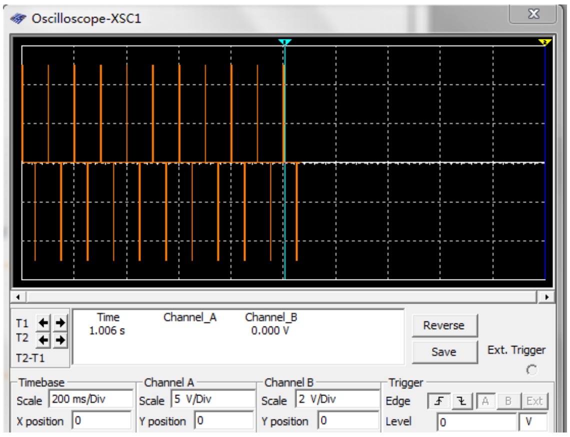
Fig. 7. Output voltage of the nano-fiber operating at 1Hz, 5Hz and 10Hz

According to the characteristics of the novel nano-fiber, it produces about 5v output voltage when operating at the frequency of 10 Hz. Therefore, the BIPOLAR_VOLTAGE module of Multisim is employed as the simulation of nano-fiber's output. The parameters of BIPOLAR_VOLTAGE module are list in Tab. 1.

Tab. 1 Parameters of BIPOLAR_VOLTAGE module

| | |
|---|---|
| Output Voltage | -5v ~ +5v |
| Frequency | 10 Hz |
| Duty Circle | 5% |

Fig. 8 shows the simulation results of the nano-fiber's output voltage.



Time 1.006 s
Channel_A
Channel_B 0.000 V

Timebase
Scale 200 ms/Div
X position 0

Channel A
Scale 5 V/Div
Y position 0

Channel B
Scale 2 V/Div
Y position 0

Trigger
Level 0 V

Fig. 8. Simulation results of the Nano-fiber's output voltage

The novel R-CMOS circuit contains a couple of CMOS units which are composed by four MOS transistors, see in Fig. 9.

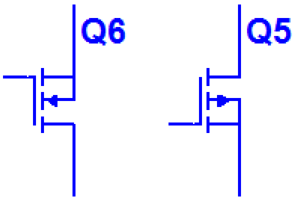
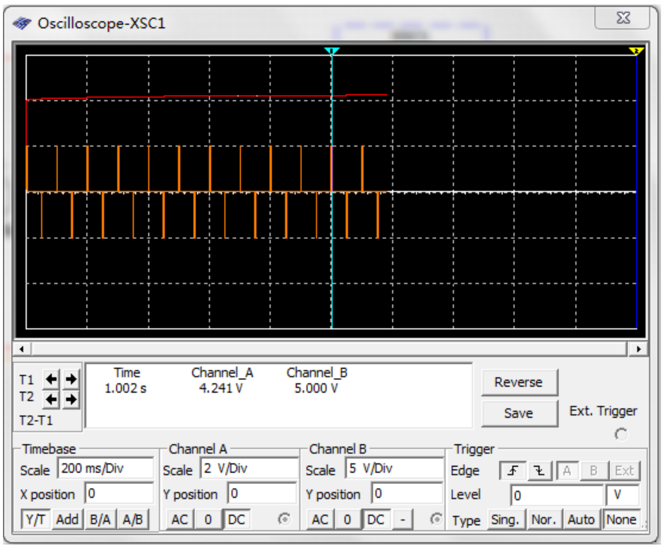


Fig. 9. pMOS and nMOS

The rectifying output voltage is archived through the switching process of N type MOS transistor and P type MOS transistor. The rectifying DC energy is then stored by a charge storage capacitor. The simulation results are shown in Fig. 10.



| Time | Channel_A | Channel_B |
|---|---|---|
| 1.002 s | 4.241 V | 5.000 V |

Timebase
Scale 200 ms/Div
X position 0

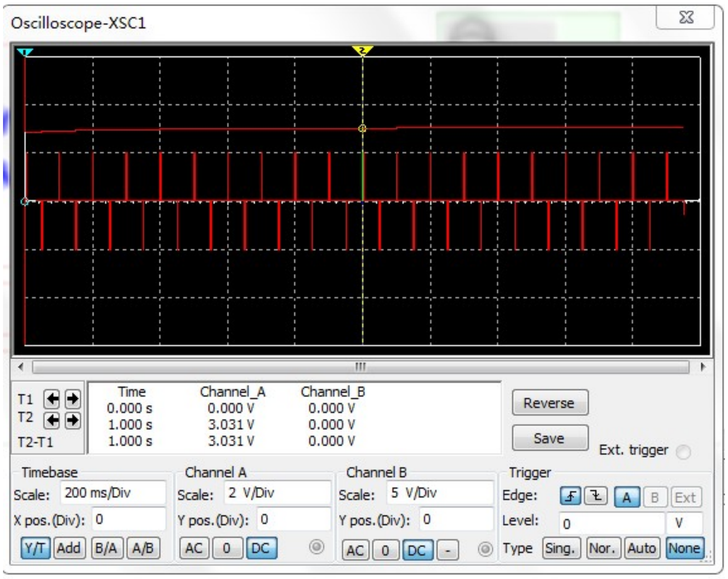
Channel A
Scale 2 V/Div
Y position 0

Channel B
Scale 5 V/Div
Y position 0

Trigger
Edge
Level 0 V
Type

Fig. 10. Simulation result of the PEH with R-CMOS rectifier

The pulse voltage in Fig. 10 shows the input (5v) of the novel harvester while the other one shows the rectifying output voltage (4.24v). The voltage can be also reflected by channel A (output voltage) and channel B (input voltage). The voltage conversion rate of the novel harvester is as high as 84.8%. Moreover, the rising time is quite short. The output reaches 4v only about 1ms. In order to justify the advantages of R-CMOS circuit in the novel harvester, the simulation result of the typical PEH with the same input voltage is displayed in Fig 11.



|  | Time | Channel_A | Channel_B |
|---|---|---|---|
| T1 | 0.000 s | 0.000 V | 0.000 V |
| T2 | 1.000 s | 3.031 V | 0.000 V |
| T2-T1 | 1.000 s | 3.031 V | 0.000 V |

Timebase
Scale: 200 ms/Div
X pos.(Div): 0

Channel A
Scale: 2 V/Div
Y pos.(Div): 0

Channel B
Scale: 5 V/Div
Y pos.(Div): 0

Trigger
Level: 0 V

Fig. 11. Simulation result of the typical PEH

Fig. 11 shows that the DC output voltage of the typical PEH circuit is about 3v. The voltage conversion rate is 60% which is much less than the PEH with R-CMOS rectifier.

## 5. CONCLUSION

The novel harvester in this paper is composed of the R-CMOS circuit which consists of four MOS transistors. A large storage capacitor is employed to store the DC energy. The novel harvester with R-CMOS rectifier has a higher voltage conversion rate than the traditional rectifier and a much lower power loss than the synchronous switch circuit. With the above advantage it performs better than the traditional rectifier circuit and the synchronous switch circuit with a low power AC source inputting. The novel harvester based on the R-CMOS circuit can be employed as a DC source for the micro sensors and wireless transducers, which will justify the potential of low power piezoelectric harvesters.

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